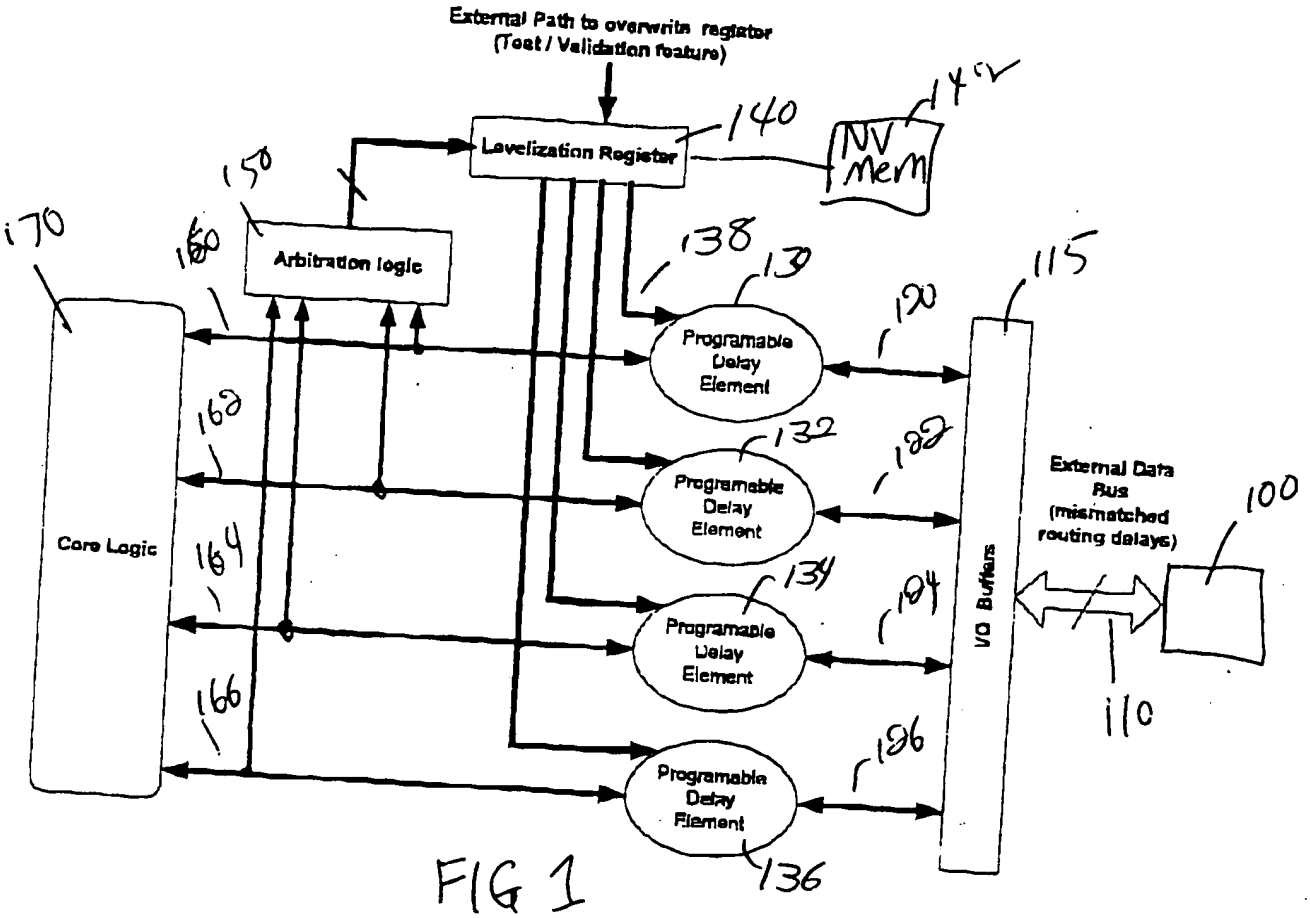
External Path to overwrite register
(Test / Validation feature)
Levelization Register
140
NV mem
Arbitration logic
150
170
160
138
130
115
120
Programable Delay Element
168
132
122
Programable Delay Element
External Data Bus
(mismatched routing delays)
100
Core Logic
164
134
124
Programable Delay Element
I/O Buffers
166
126
Programable Delay Element
136
110

FIG 1

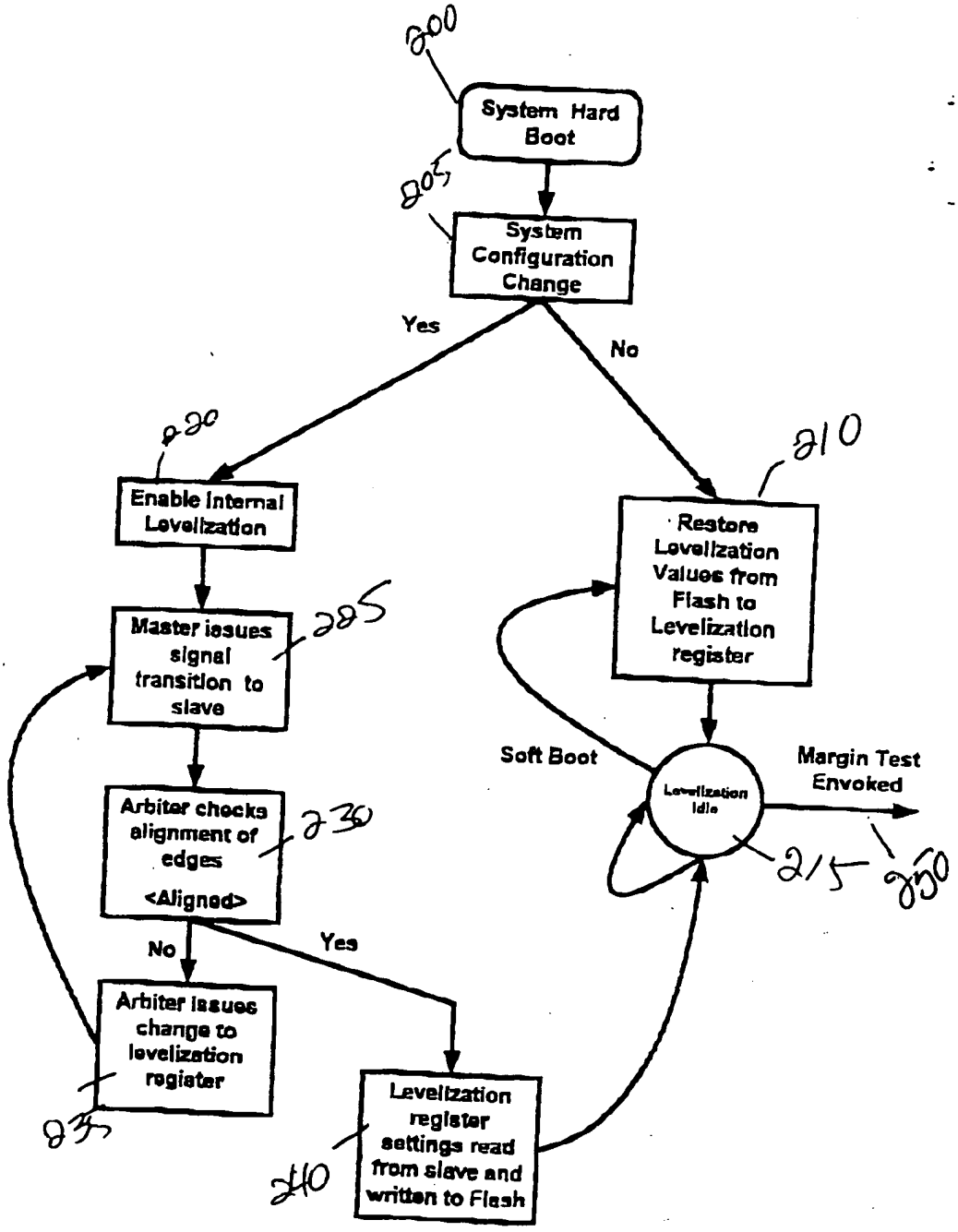
200
System Hard Boot
205
System Configuration Change
Yes
No
220
Enable Internal Levelization
210
Restore Levelization Values from Flash to Levelization register
225
Master issues signal transition to slave
Soft Boot
Levelization Idle
Margin Test Envoked
215
250
230
Arbiter checks alignment of edges
<Aligned>
No
Yes
Arbiter issues change to levelization register
235
240
Levelization register settings read from slave and written to Flash

FIG 2

System Margin Testing using line levelization registers.

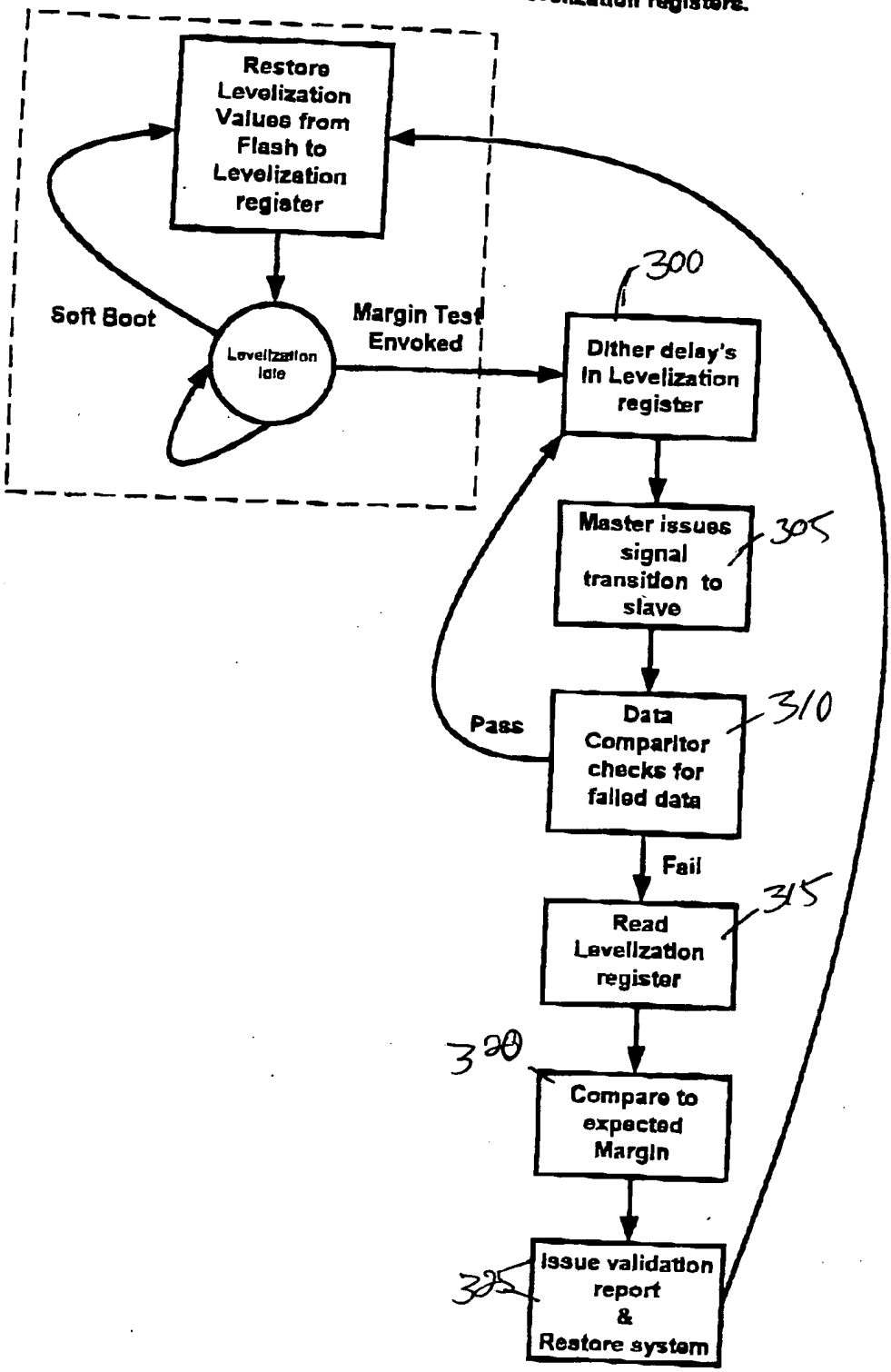

FIG3

Docket No. 42390.P15508